

3304

DUAL 16-BIT STATIC SHIFT REGISTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3304 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-Channel Enhancement Mode MOS Technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that ϕ_1 is a logic "0" and ϕ_2 is a logic "1".

ABSOLUTE MAXIMUM RATINGS (Note 1)

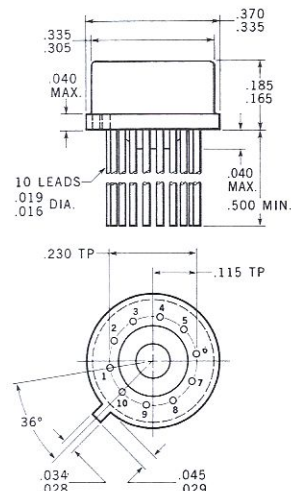
Drain Voltage (V_{DD})
Gate Voltage (V_{GG})
Clock and Data Input Voltages
Storage Temperature
Operating Temperature Range

Power Dissipation at $T_A = 25^\circ\text{C}$

—30 V to +0.3 V
—30 V to +0.3 V
—30 V to +0.3 V
—55°C to +150°C
—55°C to +85°C
0°C to +70°C
200 mW

PHYSICAL DIMENSIONS

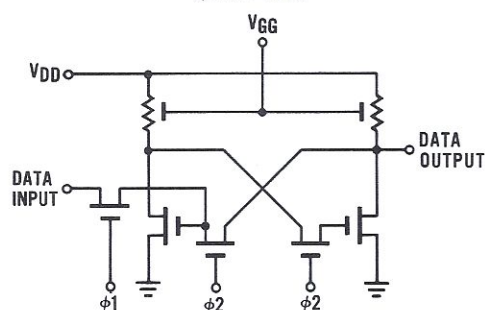
(In accordance with JEDEC TO-100)



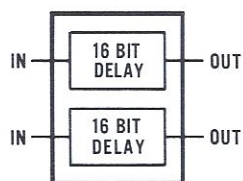
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART # A5F330414X (—55°C to +85°C)
ORDER PART # A5F330419X (0°C to +70°C)

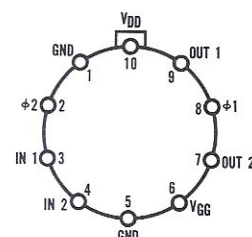
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW



NOTE:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.

*Planar is a patented Fairchild process.

MOS INTEGRATED CIRCUIT 3304

ELECTRICAL CHARACTERISTICS

($V_{DD} = -13 \text{ Volts} \pm 1 \text{ Volt}$, $V_{GG} = -27 \text{ Volts} \pm 1 \text{ Volt}$, Load = 10 M Ω and 10 pF, $T_A = -55^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Repetition Rate	D.C.		1.0	MHz	
Clock Pulse Widths					
ϕ_1 pw	0.4		10	μs	See Figure 1
ϕ_2 pw	0.4			μs	See Figure 1
Clock Delay (ϕ_d)	0.01		10	μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5.0	μs	See Figure 1
Clock Pulse Logic Levels					
(ϕ_1 & ϕ_2)					
Logic "0"			-2.0	Volts	
Logic "1"	-26		-28	Volts	
Clock Pulse Input Capacitance (ϕ_1 & ϕ_2)		4.0		pF	$\phi_1 = \phi_2 = 0 \text{ Volt}$
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2.0		pF	$V_{IN} = 0 \text{ Volt}$
Data Input Logic Levels					
Logic "0"			-2.0	Volts	
Logic "1"	-9.0			Volts	
Data Input Leakage Current			1.0	μA	$V_{IN} = -20 \text{ Volts}$
Clock Input Leakage Current			100	μA	$V_{IN} = -26 \text{ Volts}$
Clock (ϕ_2) Input Impedance	60			k Ω	$\phi_1 = -26 \text{ Volts}$ $\phi_2 = 0 \text{ Volt}$
Output Logic Levels					
Logic "0"		-0.5	-1.0	Volts	
Logic "1"	-10	-11		Volts	
Output Impedance to Ground		2.0	3.0	k Ω	Output at Logic "0"
Output Drive Capability	-5.0			Volts	$R_L = 4.0 \text{ k}\Omega$ to Ground
Power Supply Current Drain V_{DD}			10	mA	$V_{DD} = -13 \text{ Volts}$
Power Supply Current Drain V_{GG}			2.0	mA	$V_{GG} = -27 \text{ Volts}$

TIMING DIAGRAMS

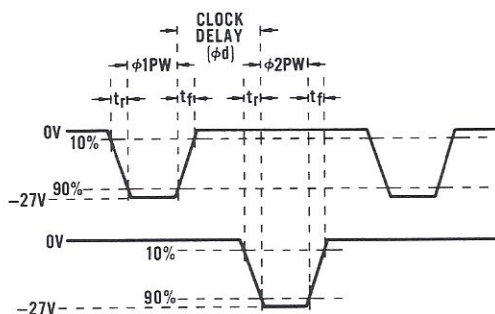


Figure 1

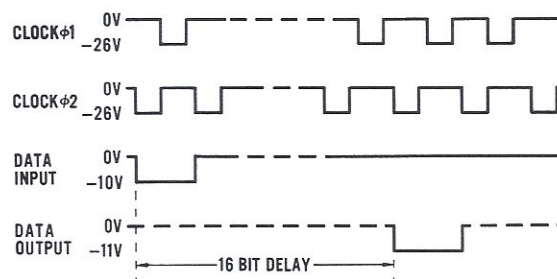
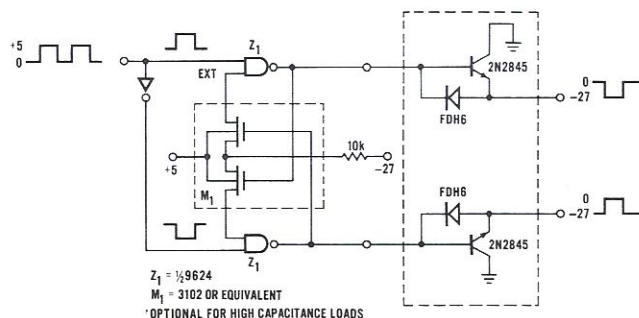


Figure 2



2 PHASE-NON-OVERLAPPING CLOCK DRIVER